IN THE CLAIMS:

1. (Currently Amended) A clock generator circuit comprising:

a phase comparator receiving a standard clock signal and an operating clock signal and generating an output signal;

a voltage controlled oscillator generating the operating clock signal based on the output signal of the phase comparator,

wherein the voltage controlled oscillator comprises:

a voltage current converter converting a voltage signal into a current signal;

a current D/A converter ~~a variable current circuit~~ fluctuating the current signal based on a digital signal; and

a current controlled oscillator oscillating the operating clock signal of which frequency corresponds to each of the variable current signals.

2. (Original) The clock generator circuit of claim 1 further comprising a first frequency dividing circuit frequency-dividing the standard clock signal and a second frequency dividing circuit frequency-dividing the operation clock signal.

3. (Currently Amended) The clock generator circuit of claim 1, wherein the ~~variable current circuit is selected from a~~ current D/A converter ~~and~~ is a current D/A converter with a low pass filter.

4. (Currently Amended) The clock generator circuit of claim 1, further comprising a control circuit controlling the ~~variable~~ current ~~circuit~~ D/A converter.

5. (Currently Amended) The clock generator circuit of claim 1, ~~wherein the variable current circuit includes~~ further comprising a determining circuit to determine the range of change of frequency of the clock oscillated by the current controlled oscillator.

6. (Currently Amended) A clock generator circuit for generating an operating clock based on a current signal generated based on a result of a comparison between a standard clock signal and a comparison clock signal comprising:

a first circuit generating a plurality of current signals ~~by changing the current signals~~; and

a second circuit generating a plurality of operating clock signals of which frequencies are different with each other based on the plurality of current signals,

wherein the first circuit comprises a current D/A converter that is controlled by a digital signal.

7. (Currently Amended) The clock generator circuit of claim 6, wherein the ~~first circuit is selected from a current D/A converter and a~~ current D/A converter ~~with~~ includes a low pass filter.

8. (Original) The clock generator circuit of claim 6 further comprising a control circuit controlling the first circuit.

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Currently Amended) A clock generator circuit comprising:

a first clock generator part generating a first clock signal, wherein the first clock generator part comprises a phase comparator for comparing a standard clock signal and an operating clock signal, a voltage current converter converting a signal based on the comparison results into a current signal and a first current controlled oscillator generating the first clock signal based on the current signal; and

a second clock generator part generating a second clock signal, wherein the second clock generator part comprises ~~a variable current circuit~~ a current D/A converter converting the current signal into variable current signals based on a digital signal and ~~the~~ a second current controlled oscillator oscillating the second clock signal of which frequency corresponds to each of the variable current signals.

13. (Currently Amended) The clock generator circuit of claim 12, wherein the ~~variable current circuit is selected from a~~ current D/A converter ~~and~~ is a current D/A converter with a low pass filter.

14. (Currently Amended) The clock generator circuit of claim 12, further comprising a control circuit controlling the ~~variable~~ current ~~circuit~~ D/A converter.

15. (Currently Amended) The clock generator circuit of claim 12, further comprising ~~wherein the variable current circuit includes~~ a determining circuit to determine the range of change of frequency of the clock oscillated by the second current controlled oscillator.

16. (Original) The clock generator circuit of claim 12, wherein the first clock generator part includes a corrective circuit that corrects the current signal and supplies the corrected current signal to the first voltage controlled oscillator.

17. (Currently Amended) A clock generator circuit ~~for~~ comprising:

a first circuit generating a first clock signal of a frequency spectrum containing N number of peaks (N is an integer) ~~comprising:~~; and

a second ~~an~~ circuit generating a second clock signal of a frequency containing a frequency spectrum with M number of peaks (~~N~~ M is an integer that is greater than 1, M>N) on the basis of a current signal generated based on ~~an~~ a comparison result of comparing a standard clock signal and an operating clock signal.

18. (Original) The clock generator circuit of claim 17, wherein the circuit includes a current D/A converter or a current D/A converter with a low pass filter to fluctuate the current signal.

19. (Currently Amended) A PLL circuit comprising:

a phase comparator receiving and comparing a standard clock signal and an operating clock signal;

a charge pump supplying an output signal based on the comparison;

a voltage controlled oscillator outputting the operating clock signal based on the output signal of the charge pump;

wherein the voltage controlled oscillator comprises a voltage current converter that converts a voltage signal into a current signal;

a current D/A converter ~~variable current circuit~~ that changes the current signal into a variable current signal based on a digital signal; and

a current controlled oscillator that oscillates the operating clock signal based on the variable current signal.

20. (Currently Amended) A clock generation method comprising the steps of:

comparing a standard clock signal and an operating clock signal;

converting the results of the comparison into a current signal;

using a current D/A converter to change ~~changing~~ the current signal into variable current signals based on a digital control signal; and

outputting the operating clock signal with varying frequencies based on the variable current signal.

21. (Canceled)

22. (Canceled)